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Intel Ref.: P12891

REMARKS

Claims 1 to 30 are pending in the application. Claims 1, 9, 11, 19, 21 and 29 are independent. Favorable reconsideration and further examination are respectfully requested.

Claim 9 was objected to for not containing an "intended use or purpose" in the preamble. Applicants have amended the preamble to claim 9 to state an intended use or purpose of the invention. Accordingly, withdrawal of the objection is respectfully requested.

Claims 1 to 30 were rejected under 35 U.S.C. § 102(b) over U.S. Patent No. 5,220,512 (Watkins). As shown above, Applicants have amended the claims to define the invention with greater clarity. In view of these clarifications, reconsideration and withdrawal of the art rejection are respectfully requested.

Amended independent claim 1 defines a method of modeling a logic design, which comprises creating a graphical representation of the logic design, receiving a selection that corresponds to a type of simulation code, generating simulation code based on the graphical representation and the selection, where the simulation code is executable code, and using the simulation code to test the operation of the logic design.

The applied art is not understood to disclose or to suggest the foregoing features of claim 1, particularly with respect to generating executable simulation code and to using the simulation code to test the operation of the logic design.

Watkins describes a system for simulating circuit designs. The Watkins system stores, in a database, software models that define the operation of corresponding circuit elements. Using a list of such components and associated connections as input, the Watkins system applies a logic

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compiler to output schematic object files. A logic simulator then utilizes the schematic object files and software models to produce simulation results based on initial conditions and signal values. What Watkins does not disclose, however, is the generation of executable simulation code.

Furthermore, claim 1 includes a logic testing approach not suggested in Watkins. The Watkins system discloses a logic verifier to check the schematic object files produced by the logic compiler for interconnection errors. Watkins' logic verifier reveals errors, such as outputs connected together, by checking the design against rules stored in a component database. However, Watkins fails to teach the use of the simulation code to test the operation of the logic design. For at least these reasons, Applicants submit that claim 1 is patentable over Watkins.

Amended independent claims 11 and 21 are article of manufacture and apparatus claims, respectively, that roughly correspond to claim 1. These claims are also believed to be allowable for at least the same reasons noted above with respect to claim 1.

Amended independent claim 9 defines a method that includes displaying a menu comprised of different types of functional block diagrams, receiving an input selecting one of the different types of functional block diagrams, receiving a selection that corresponds to a type of simulation code, retrieving a selected functional block diagram, creating a graphical representation of a logic design using the selected functional block diagram, generating simulation code to simulate operation of the logic design based on the graphical representation and the selection, wherein the simulation code is executable code, and using the simulation code to test the operation of the logic design. Creating the graphical representation of the logic design

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includes interconnecting the selected functional block diagram with one or more other functional block diagrams to generate a model of a logic design, and defining the selected functional block diagram using the type of simulation code if a function of the functional block diagram is undefined when retrieved.

The applied art is not understood to disclose or to suggest the foregoing features of claim 9. More specifically, as explained above with respect to claim 1, Watkins does not disclose or suggest either the generation of executable simulation code or the logic testing of the simulation code. Accordingly, Watkins could not possibly anticipate, or render obvious, the elements of claim 9 that include, or depend on, such features. Claim 9 is therefore believed to be patentable over Watkins.

Amended independent claims 19 and 29 are article of manufacture and apparatus claims, respectively, that roughly correspond to claim 9. These claims are also believed to be allowable for at least the same reasons noted above with respect to claim 9.

Each of the dependent claims is also believed to define patentable features of the invention. Each dependent claim partakes of the novelty of its corresponding independent claim and, as such, has not been discussed specifically herein.

It is believed that all of the pending claims have been addressed. However, the absence of a reply to a specific rejection, issue or comment does not signify agreement with or concession of that rejection, issue or comment. In addition, because the arguments made above may not be exhaustive, there may be reasons for patentability of any or all pending claims (or other claims) that have not been expressed. Finally, nothing in this paper should be construed as

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an intention to concede any issue with regard to any claim, except as specifically stated in this paper, and the amendment of any claim does not necessarily signify concession of unpatentability of the claim prior to its amendment.

In view of the foregoing amendments and remarks, Applicants respectfully submit that the application is in condition for allowance, and such action is respectfully requested at the Examiner's earliest convenience.

Applicants' undersigned attorney can be reached at the address shown below. All telephone calls should be directed to the undersigned at 617-521-7896.

No additional fees are believed to be due for this Amendment; however, if any fees are due, please charge them to deposit account 06-1050, referencing Attorney Docket No. 10559-607001.

Respectfully submitted,

Date: June 15, 2005

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